

IN THE CLAIMS

Please amend the claims as follows.

1. (Canceled)
2. (Previously Presented) A capacitor, comprising:
 - a first electrode;
 - a second electrode;
 - a single compound, dielectric layer interposed between the first electrode and the second electrode;
 - a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and one of the first and second electrodes; and
 - wherein the one electrode is a tungsten nitride and the buffer layer is a tungsten oxide.
3. (Original) The capacitor according to claim 2, wherein the dielectric layer is a tantalum oxide.
4. (Canceled)
5. (Previously Presented) A capacitor, comprising:
 - a first electrode;
 - a second electrode;
 - a dielectric layer interposed between the first electrode and the second electrode; and
 - a tungsten trioxide buffer layer interposed between and directly adjoining the dielectric layer and one of the first and second electrodes.
6. (Original) The capacitor according to claim 5, wherein the buffer layer has a orthorhombic crystalline structure.

7. (Original) The capacitor according to claim 5, wherein the one electrode includes tungsten.

8. (Original) The capacitor according to claim 7, wherein the buffer layer is grown by oxidizing the one electrode.

9. – 12. (Canceled)

13. (Previously Presented) A vertical capacitor, comprising:

- a bottom electrode;
- a top electrode positioned above the bottom electrode;
- a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and
- a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and the bottom electrode, wherein the bottom electrode is a tungsten nitride and the buffer layer is a tungsten oxide.

14. (Original) The capacitor according to claim 13, wherein the dielectric layer is a tantalum oxide.

15. (Previously Presented) A vertical capacitor, comprising:

- a bottom electrode;
- a top electrode positioned above the bottom electrode;
- a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and
- a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and the bottom electrode, wherein the buffer layer has a orthorhombic crystalline structure.

16. (Previously Presented) A capacitor, comprising:

a bottom electrode;

a top electrode;

a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and

a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and the bottom electrode, wherein the metal in the buffer layer is a refractory metal.

17. (Original) The capacitor according to claim 16, wherein the metal in the buffer layer is tungsten.

18. (Original) The capacitor according to claim 17, wherein the bottom electrode comprises a metal nitride, and the metal in the bottom electrode is a refractory metal.

19. (Original) The capacitor according to claim 18, wherein the bottom electrode comprises tungsten nitride.

20. (Previously Presented) A capacitor, comprising:

a bottom electrode;

a top electrode;

a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and

a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and the bottom electrode, wherein the bottom electrode comprises a metal nitride having a metal component which is the same as the metal component of the metal oxide buffer layer.

21. (Original) The capacitor according to claim 20, wherein the dielectric layer comprises tantalum oxide.

22. (Original) The capacitor according to claim 21, wherein the metal component of the bottom electrode and the buffer layer includes tungsten.

23. (Previously Presented) A capacitor, comprising:

a bottom electrode;

a top electrode;

a single compound, dielectric layer interposed between the bottom electrode and the top electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the bottom electrode and the top electrode;

wherein at least one electrode selected from the group consisting of the bottom electrode and the top electrode comprises tungsten nitride.

24. (Original) The capacitor according to claim 23, wherein the dielectric layer is a metal oxide of a different type than the buffer layer.

25. (Previously Presented) A capacitor, comprising:

a first electrode;

a second electrode;

a single compound, tantalum oxide dielectric layer interposed between the bottom electrode and the top electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the bottom electrode and the top electrode;

wherein at least one electrode is selected from the group consisting of the bottom electrode and the top electrode includes tungsten nitride.

26. (Previously Presented) A capacitor, comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and one of the first and second electrodes, wherein the metal oxide buffer layer has an orthorhombic crystal structure, and wherein the metal in the buffer layer is tungsten.

27. – 28. (Canceled)

29. (Previously Presented) The capacitor according to claim 16, wherein the bottom electrode comprises a metal nitride and has a metal component which is the same as the metal component of the metal oxide buffer layer.

30. (Previously Presented) A capacitor, comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode;

a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and one of the first and second electrodes;

wherein the buffer layer has a dielectric constant greater than the dielectric layer; and

wherein the one of the first and second electrodes has a metal component which is the same as the metal component of the buffer layer.

31. (Canceled)

32. (Original) The capacitor according to claim 30, wherein the buffer layer has an orthorhombic crystalline structure.

33-73. (Canceled)

74. (Previously Presented) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode.

75. (Previously Presented) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

wherein at least one electrode selected from the group consisting of the first electrode and the second electrode comprises tungsten nitride.

76. (Previously Presented) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a tungsten nitride second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

a tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and the second electrode.

77. (Previously Presented) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a tungsten nitride second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

a high temperature annealed, tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and the second electrode.

78. (Original) The semiconductor die according to claim 77, wherein the high temperature annealed buffer layer is annealed at least 700 degrees Celsius and has an orthorhombic crystal structure.

79. (Canceled)

80. (Previously Presented) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode;

a metal oxide buffer layer is interposed between and directly adjoining the dielectric layer and the second electrode,

wherein the buffer layer has a dielectric constant greater than the dielectric layer;

and

wherein the electrode selected from the group consisting of the first electrode and the second electrode has a metal component that is the same as the metal component of the buffer layer.

81.-82. (Canceled)

83. (Previously Presented) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

84. (Previously Presented) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, wherein at least one electrode selected from the group consisting of the bottom electrode of the capacitor and the top electrode of the capacitor comprises tungsten nitride;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

85. (Canceled)

86. (Previously Presented) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having a dielectric constant greater than the dielectric layer, wherein an electrode selected from the group consisting of the first electrode and the second electrode includes a metal component that is the same as the metal component of the buffer layer;

a row access circuit coupled to the array of memory cells;
a column access circuit coupled to the array of memory cells; and
an address decoder circuit coupled to the row access circuit and the column access circuit.

87. - 89. (Canceled)

90. (Previously Presented) A memory module, comprising:

a support;
a plurality of leads extending from the support;
a command link coupled to at least one of the plurality of leads;
a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;
a second electrode;
a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;
a column access circuit coupled to the array of memory cells; and
an address decoder circuit coupled to the row access circuit and the
column access circuit.

91. (Previously Presented) A memory module, comprising:

a support;
a plurality of leads extending from the support;
a command link coupled to at least one of the plurality of leads;
a plurality of data links, wherein each data link is coupled to at least one of the plurality
of leads; and

at least one memory device contained on the support and coupled to the command link,
wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a
capacitor, the capacitor comprising:

a first electrode;
a second electrode;
a single compound, metal oxide dielectric layer interposed between
the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten
oxide buffer layer is interposed between and directly adjoining the dielectric layer and an
electrode selected from the group consisting of the first electrode and the second electrode, the
buffer layer having a dielectric constant greater than the dielectric layer;

a row access circuit coupled to the array of memory cells;
a column access circuit coupled to the array of memory cells; and
an address decoder circuit coupled to the row access circuit and the
column access circuit wherein at least one electrode selected from the group consisting of the
bottom electrode of the capacitor and the top electrode of the capacitor comprises tungsten
nitride.

92. - 95. (Canceled)

96. (Previously Presented) A memory system, comprising:

- a controller;

- a command link coupled to the controller;

- a data link coupled to the controller; and

- a memory device coupled to the command link and the data link, wherein the memory device comprises:

- an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

- a first electrode;

- a second electrode;

- a single compound, dielectric layer interposed between the first electrode and the second electrode; and

- at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

- a row access circuit coupled to the array of memory cells;

- a column access circuit coupled to the array of memory cells; and

- an address decoder circuit coupled to the row access circuit and the column access circuit.

97. (Canceled)

98. (Previously Presented) A memory system, comprising:

- a controller;

- a command link coupled to the controller;

- a data link coupled to the controller; and

- a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having a dielectric constant greater than the dielectric layer, wherein the electrode selected from the group consisting of the first electrode and the second electrode includes a metal component that is the same as the metal component of the buffer layer;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

99. - 101. (Canceled)

102. (Previously Presented) An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode.

103. (Canceled)

104. (Previously Presented) An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the bottom electrode and the top electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, wherein the electrode selected from the group consisting of the first electrode and the second electrode includes a metal component that is the same as the metal component of the buffer layer;

wherein the metal oxide buffer layer has a dielectric constant greater than the dielectric constant of the dielectric layer.

105. (Canceled)

106. (Previously Presented) A capacitor, comprising:

an annealed bottom electrode;

a top electrode;

a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and

an annealed metal oxide buffer layer intermediate and directly adjoining the dielectric layer and the bottom electrode.

107. - 110. (Canceled)

111. (Previously Presented) A memory cell comprising a capacitor and an access device, wherein the capacitor includes:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode;

a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and one of the first and second electrodes; and

wherein the one electrode is a tungsten nitride and the buffer layer is a tungsten oxide.

112. (Canceled)

113. (Previously Presented) A memory cell comprising a capacitor and an access device, wherein the capacitor includes:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a tungsten trioxide buffer layer interposed between and directly adjoining the dielectric layer and one of the first and second electrodes.

114. (Original) The memory cell according to claim 113, wherein the one electrode includes tungsten.

115. (Original) The memory cell according to claim 114, wherein the buffer layer is grown by oxidizing the one electrode.

116. - 118. (Canceled)

119. (Previously Presented) A processor and a memory cell electrically connected to said processor, wherein said memory cell includes a capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode;

a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and one of the first and second electrodes; and

wherein the one electrode is a tungsten nitride and the buffer layer is a tungsten oxide.

120. (Canceled)

121. (Previously Presented) A processor and a memory cell electrically connected to said processor, wherein said memory cell includes a capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

a tungsten trioxide buffer layer interposed between and directly adjoining the dielectric layer and one of the first and second electrodes.

122. (Original) The memory cell according to claim 121, wherein the one electrode includes tungsten.

123. (Original) The memory cell according to claim 122, wherein the buffer layer is grown by oxidizing the one electrode.

124-126. (Canceled)

127. (Previously Presented) The capacitor of claim 2, wherein the dielectric layer comprises a single layer.

128. (Previously Presented) The capacitor of claim 26, wherein the metal oxide buffer layer includes tungsten.

129. (Previously Presented) The capacitor of claim 128, wherein the bottom electrode includes a nitride.

130. (Previously Presented) The capacitor of claim 128, wherein the bottom electrode includes tungsten nitride.

131. (Previously Presented) The capacitor of claim 26, wherein the bottom electrode comprises a metal nitride and has a metal component which is the same as the metal component of the metal oxide buffer layer.

132. (Previously Presented) The capacitor of claim 26, wherein the dielectric layer comprises a single layer.

133. (Previously Presented) The capacitor of claim 26, wherein the buffer layer is of the formula MO_x , and M is a metal component from a group consisting of tantalum, zirconium, and hafnium.

134. (Previously Presented) The capacitor of claim 30, wherein the dielectric layer comprises a single layer.

135. (Previously Presented) The capacitor of claim 30, wherein the metal oxide buffer layer includes tungsten.

136. (Previously Presented) The capacitor of claim 30, wherein the second electrode includes a nitride.

137. (Previously Presented) The capacitor of claim 30, wherein the second electrode includes tungsten nitride.

138. (Previously Presented) The capacitor of claim 30, wherein the second electrode comprises a metal nitride and has a metal component which is the same as the metal component of the metal oxide buffer layer.

139. -140. (Canceled)

141. (Currently Amended) ~~The semiconductor die of claim 79,~~ A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode;

a metal oxide buffer layer is interposed between and directly adjoining the dielectric layer and the second electrode, wherein the buffer layer has an orthorhombic crystal lattice structure, and wherein the metal oxide buffer layer includes tungsten; and

wherein the electrode selected from the group consisting of the first electrode and the second electrode has a metal component that is the same as the metal component of the buffer layer.

142. (Canceled)

143. (Currently Amended) ~~The semiconductor die of claim 79,~~ A semiconductor die,
comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit
devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor,
the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the
second electrode;

a metal oxide buffer layer is interposed between and directly adjoining the
dielectric layer and the second electrode, wherein the buffer layer has an orthorhombic crystal
lattice structure, and wherein the metal oxide buffer layer includes tungsten; and

wherein the electrode selected from the group consisting of the first electrode and the
second electrode has a metal component that is the same as the metal component of the buffer
layer; wherein the second electrode includes tungsten nitride.

144. - 146. (Canceled)

147. (Previously Presented) The semiconductor die of claim 80, wherein the dielectric layer
comprises a single layer.

148. (Previously Presented) The semiconductor die of claim 80, wherein the metal oxide
buffer layer includes tungsten.

149. (Previously Presented) The semiconductor die of claim 80, wherein the second electrode
includes a nitride.

150. (Previously Presented) The semiconductor die of claim 80, wherein the second electrode
includes tungsten nitride.

151. (Previously Presented) The semiconductor die of claim 80, wherein buffer layer includes tantalum.

152. (Previously Presented) The semiconductor die of claim 80, wherein buffer layer includes zirconium.

153. (Previously Presented) The semiconductor die of claim 80, wherein buffer layer includes hafnium.